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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/876,396	06/07/2001	Syuuichi Kariyazaki	14701	7345

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EXAMINER	
OWENS, DOUGLAS W	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 08/31/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/876,396	KARIYAZAKI, SYUUICHI	
	Examiner	Art Unit	
	Douglas W. Owens	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 August 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1 – 10 are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent No. 5,77,383 to Stager et al.

Regarding claim 1, Stager et al. teach a semiconductor device (Figs. 1 & 2, for example) comprising:

a semiconductor member (14) having thereon a plurality of electrode terminals; and

a mounting member having a plurality of interconnect pads (12) electrically and mechanically connected to the respective electrode terminals for mounting the semiconductor member on the mounting member; and

the interconnect pads forming a plurality of I/O cells including signal terminals, (Col. 3, lines 47 – 57), the I/O cells forming a first group of the I/O cells and a second group of I/O cells on an inner position of the mounting member with respect to the first group.

Regarding claim 2, Stager et al. teach a semiconductor device, wherein the semiconductor member is a semiconductor chip, the electrode terminals are internal

electrodes disposed on a bottom surface of the semiconductor chip, and the mounting member is a package substrate used for packaging thereon the semiconductor chip.

Regarding claim 3, Stager et al. teach a semiconductor device, wherein the mounting member is a semiconductor package for mounting the semiconductor chip member on a mounting substrate, the semiconductor package includes ball electrodes (Fig. 5) disposed on a bottom surface of a packaging substrate, and the mounting substrate forms a specified circuit by mounting the semiconductor package thereon.

Regarding claim 4, Stager et el. teach a semiconductor device that would have inherently included terminals for power and ground since they are required for device operation.

Regarding claim 5, Stager et al. teach a semiconductor device, wherein the I/O cells would have inherently included peripherals, since the purpose of the terminals and interconnection is for connection to peripheral devices.

Regarding claim 6, Stager et al. teach a semiconductor device, herein an interconnect line (16) is electrically connected to each of the interconnect pads and the interconnect lines electrically connected to the interconnect pads of at least one of the I/O cells are formed in a single interconnect layer.

Regarding claim 7, Stager et al. teach a semiconductor device, wherein the interconnect pads and the interconnect lines electrically connected to the interconnect pads in the single interconnect layer are formed on the surface of a packaging substrate. Since it can be seen that the interconnect lines extend to the surface for electrical connection to the pads (12) they are considered to be formed on the surface.

Regarding claim 8, Stager et al. teach a semiconductor device, wherein the interconnect lines connected to the I/O cells located on inner positions extend between the I/O cells located on an outer periphery (Fig. 1).

Regarding claim 9, Stager et al. teach a semiconductor device, wherein the interconnect pads and the interconnect lines (16, 18, 20, 22) electrically connected to the interconnect pads are formed as a multi-layered interconnect layer in the substrate.

Regarding claim 10, Stager et al. teach a semiconductor device, wherein at least one of the first group and the second group includes an outer group and inner group disposed on the inner position of the mounting member with respect to the outer group (Fig. 2).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Stager et al. as applied to claims 1 – 10 above, and further in view of US Patent No. 6,271,478 to Horiuchi et al.

Stager et al. do not teach a semiconductor device, wherein the interconnect lines electrically connected to the interconnect pads corresponding to eh first group of I/O cells and interconnect lines electrically connected to the interconnect pads

corresponding to the second group of I/O cells are formed in different interconnect layers. Horiuchi et al. teach a semiconductor device, wherein the interconnect lines electrically connected to the interconnect pads corresponding to eh first group of I/O cells and interconnect lines electrically connected to the interconnect pads corresponding to the second group of I/O cells are formed in different interconnect layers (Fig. 13). It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teaching of Horiuchi et al. into the device taught by Stager et al. since it is desirable to decrease the number of circuit boards for mounting an electronic part (Col. 3, lines 43 – 49).

Conclusion

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Douglas W. Owens whose telephone number is 571-272-1662. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Douglas W Owens
Primary Examiner
Art Unit 2811

DWO
August 24, 2006